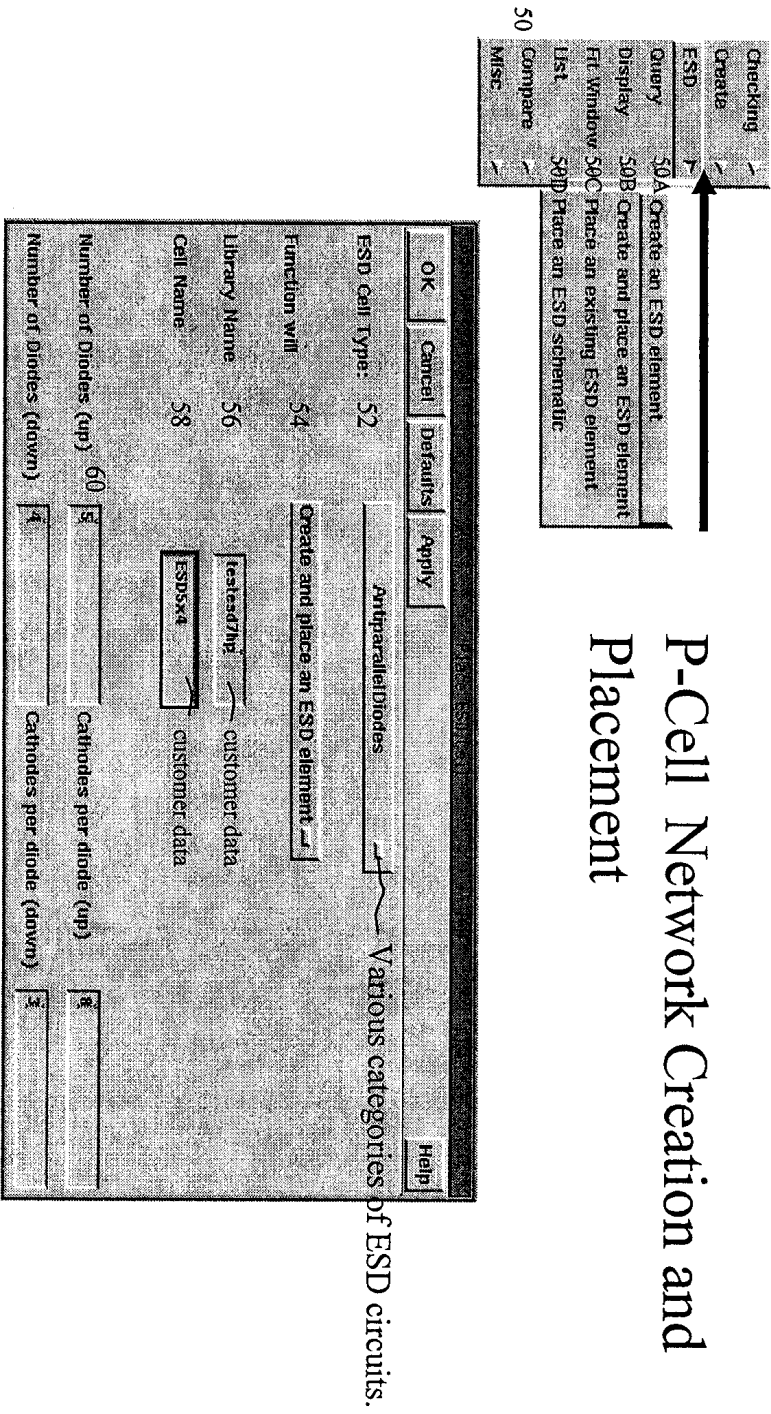


Figure 1

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P-Cell Network Creation and Placement



P-Cell Schematic and Graphical Representation

Symbol Function

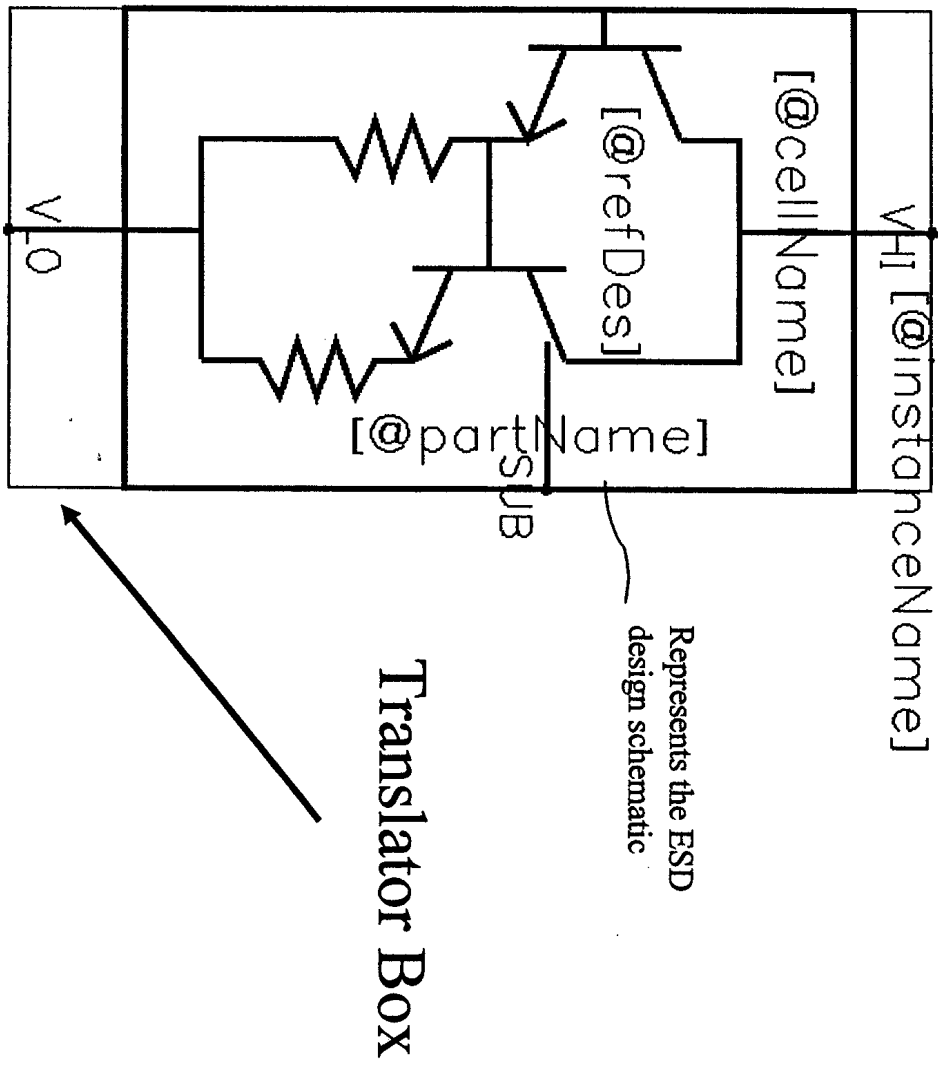


Figure 3

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Symbol Placement in Schematic Design

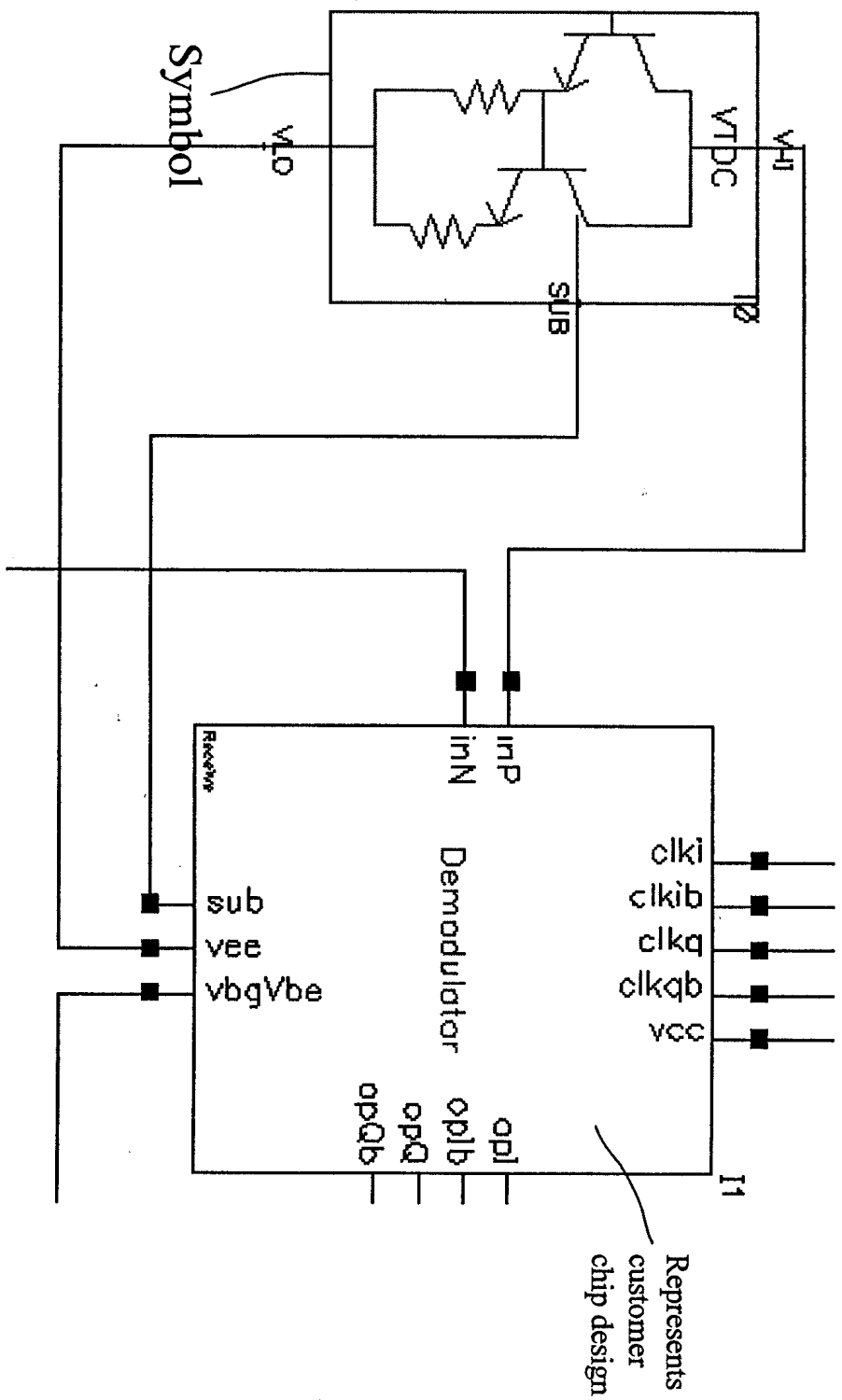


Figure 4

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Schematic Representation of Hierarchical Circuit

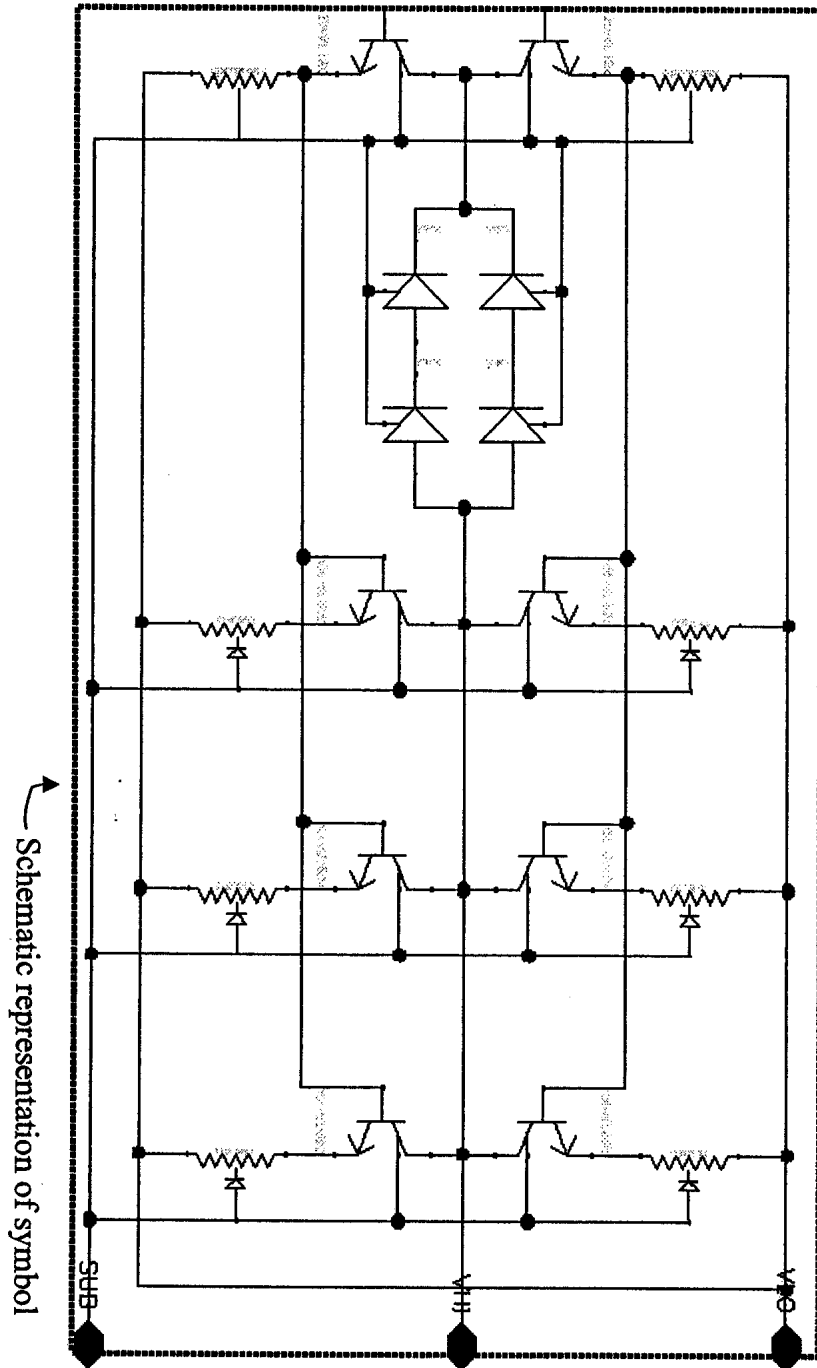


Figure 5

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Hierarchical Schematic Placement in Design Schematics

Schematic representation of ESD

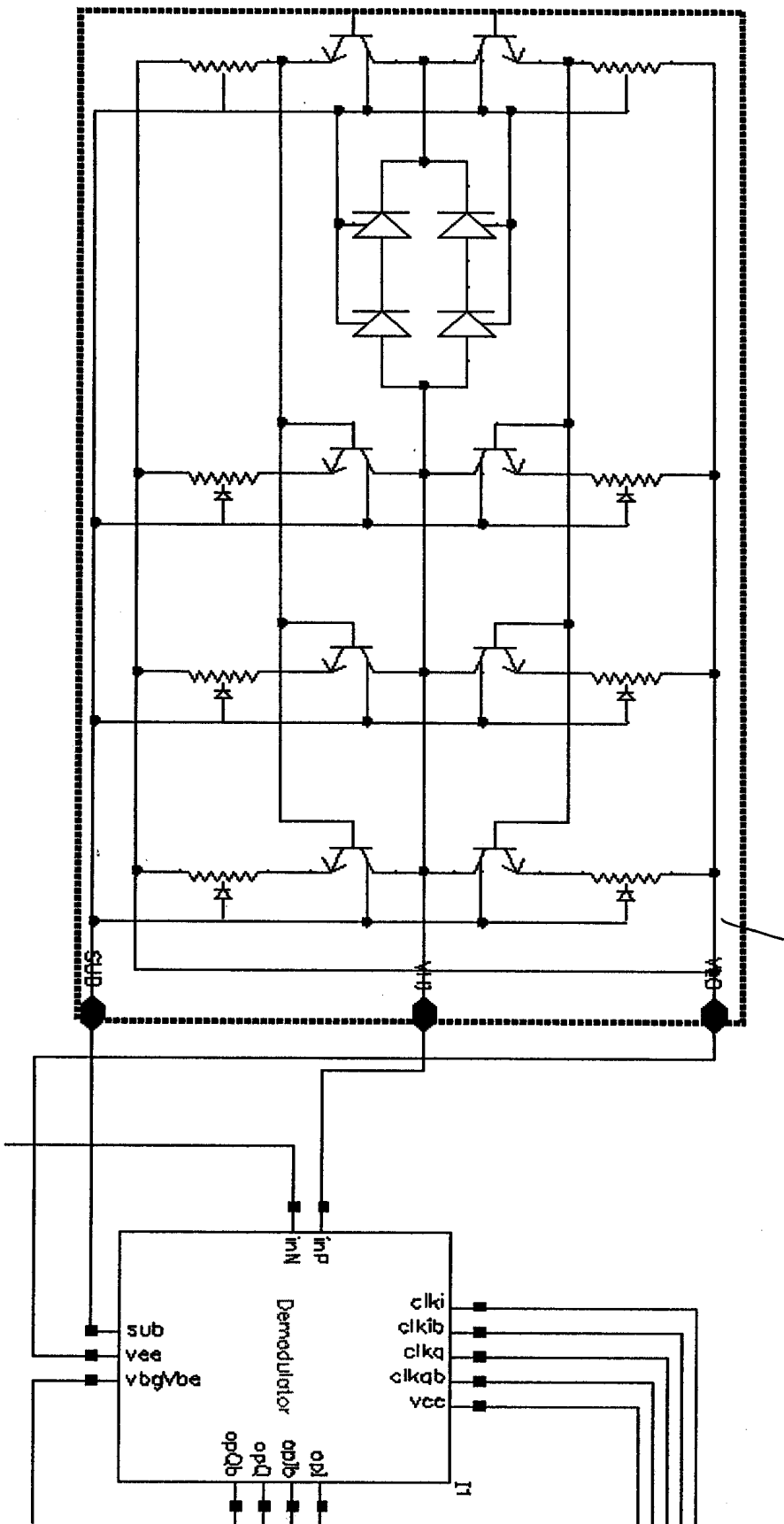
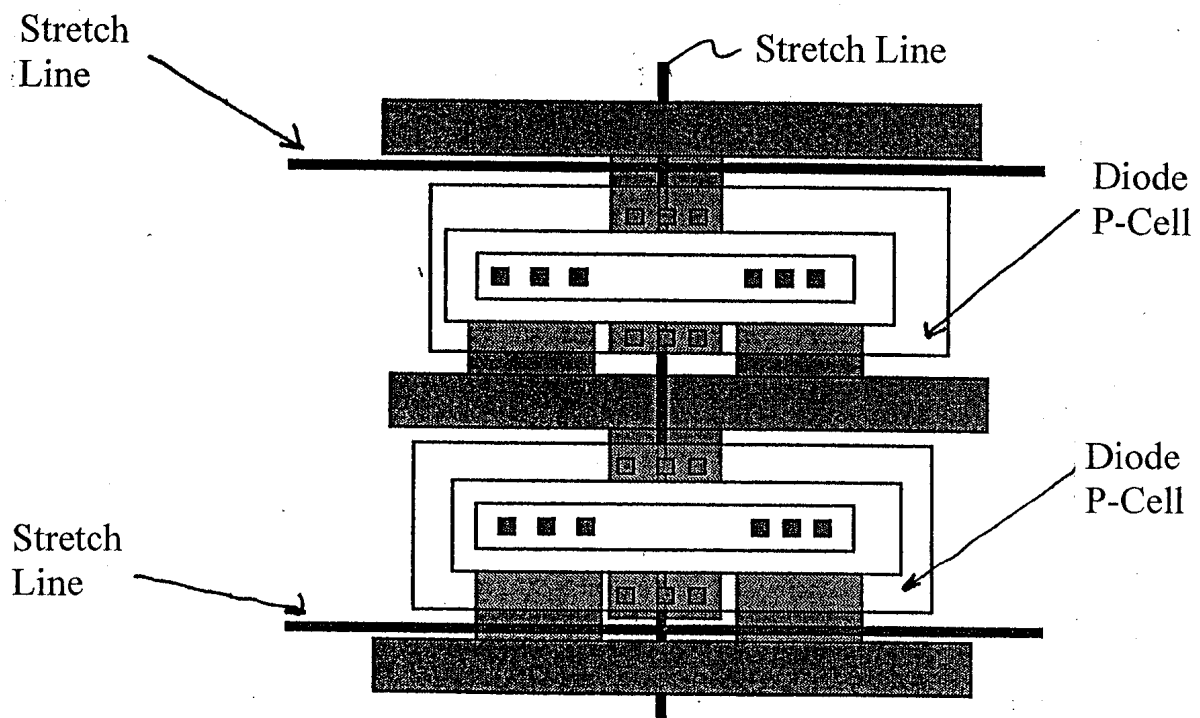


Figure 6

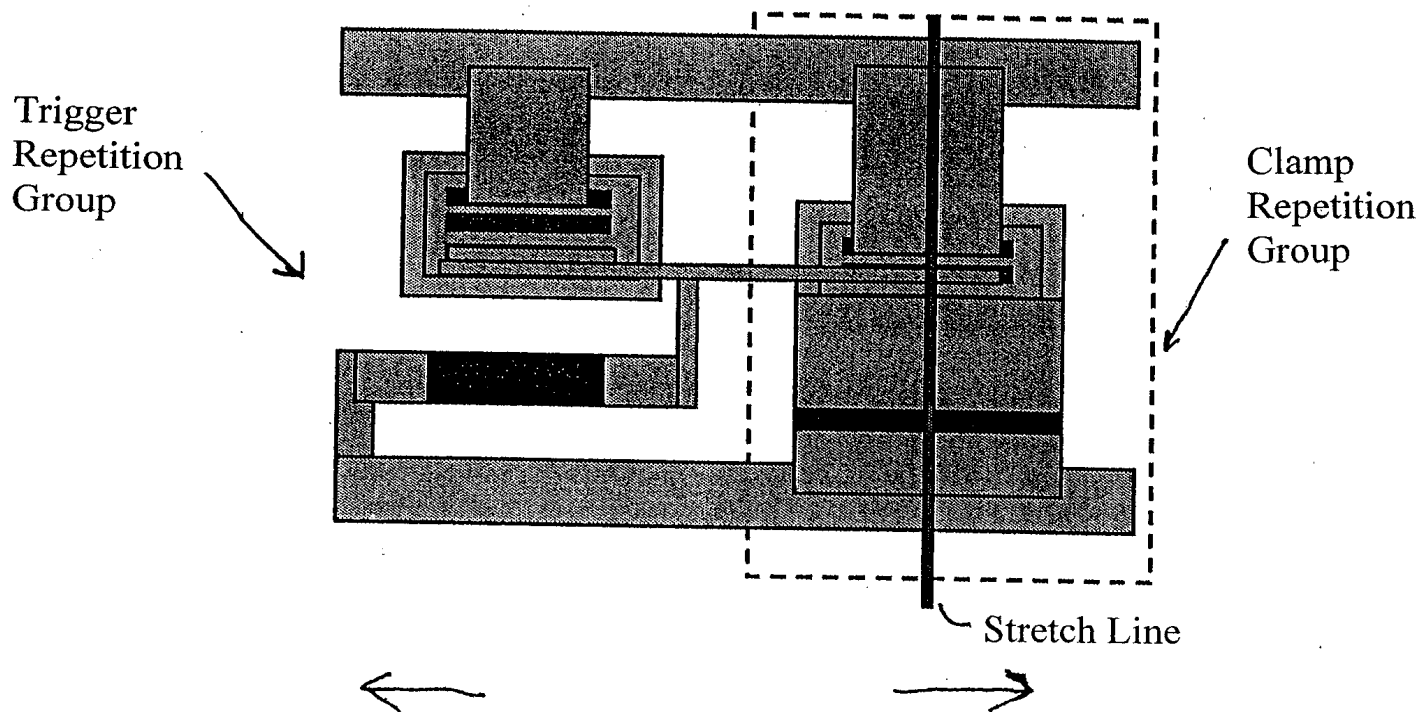
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Figure 7



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Figure 8



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Graphical Representation of Hierarchical Design

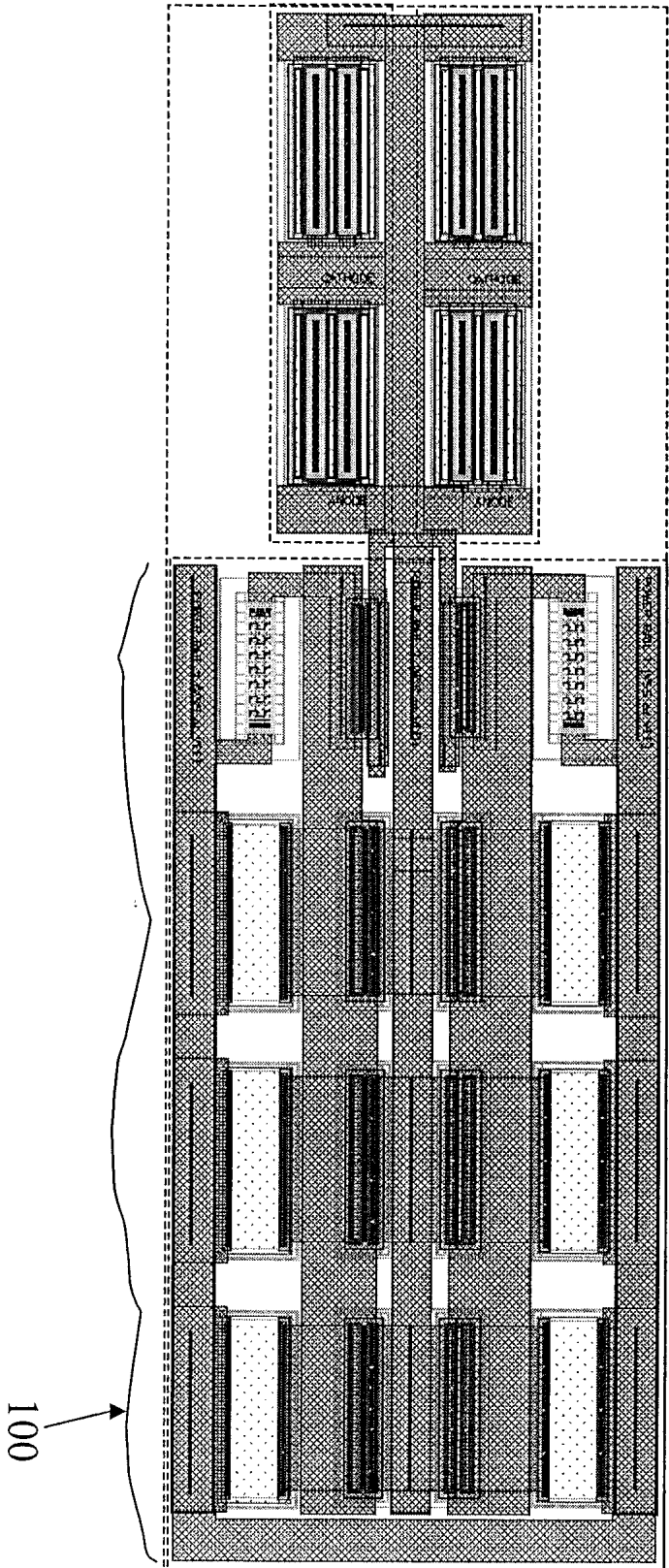
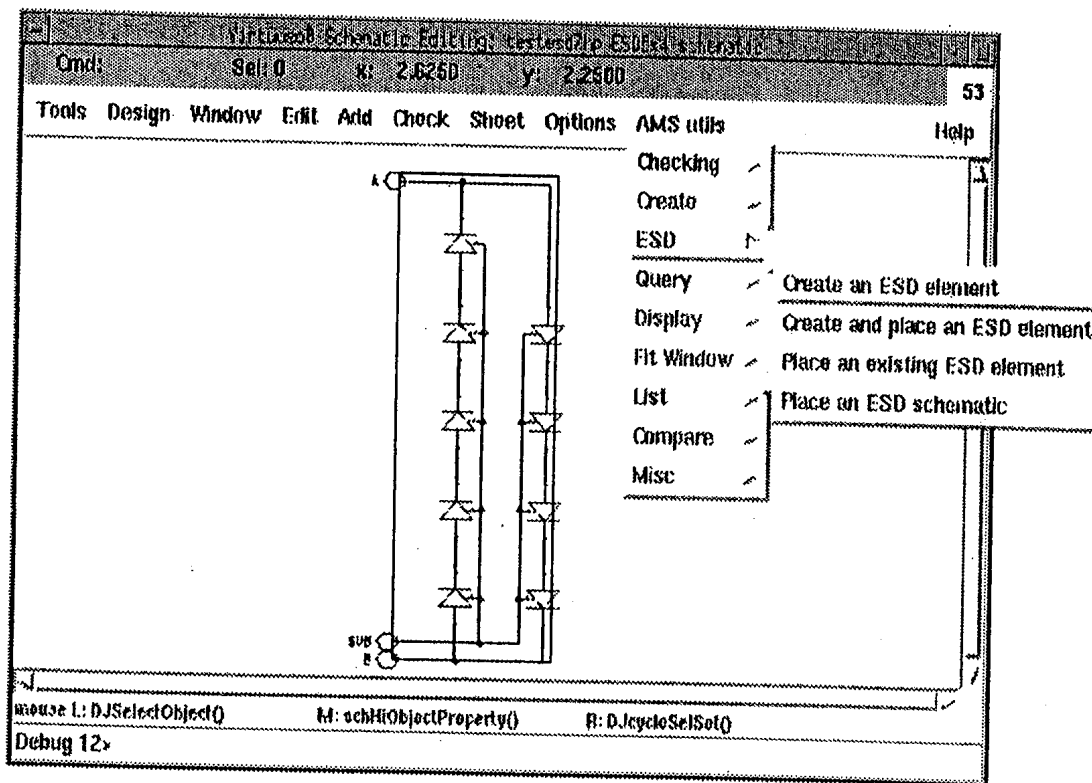


Figure 9

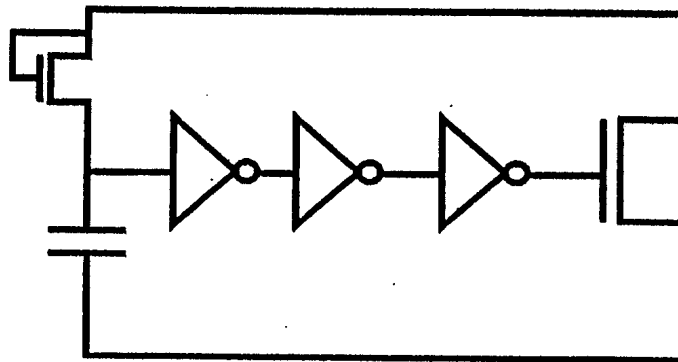
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Figure 10



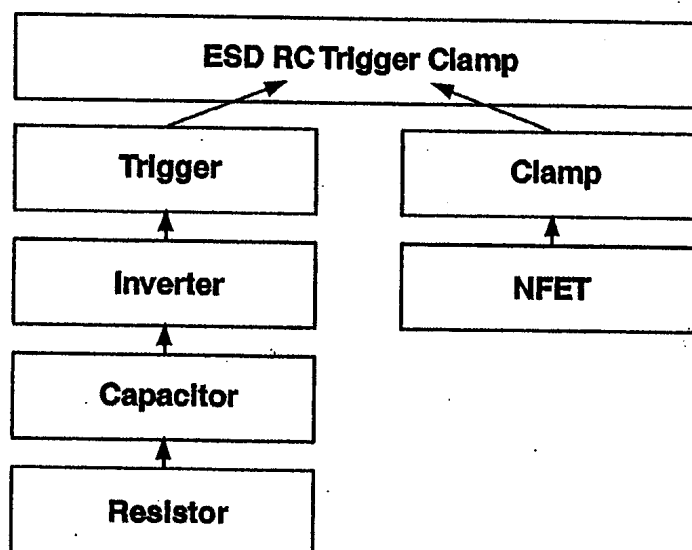
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Figure 11



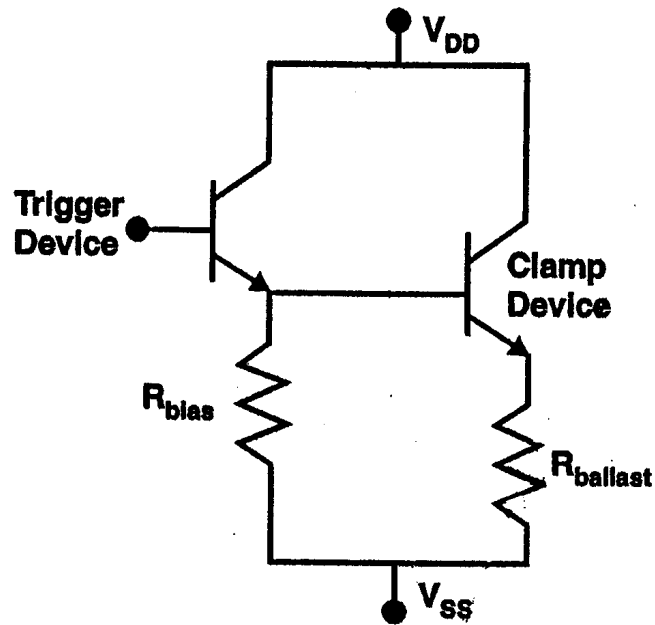
Symbol for D-C trigger clamp

Figure 12



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Figure 13



Symbol representation
Variations of styles –
for type of ESD element

Figure 14

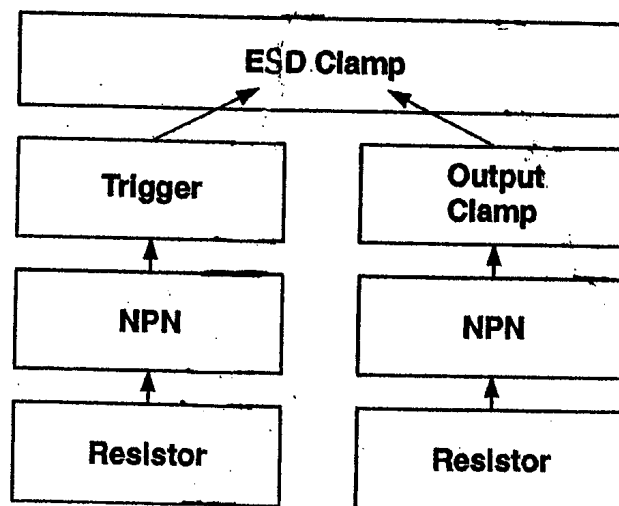
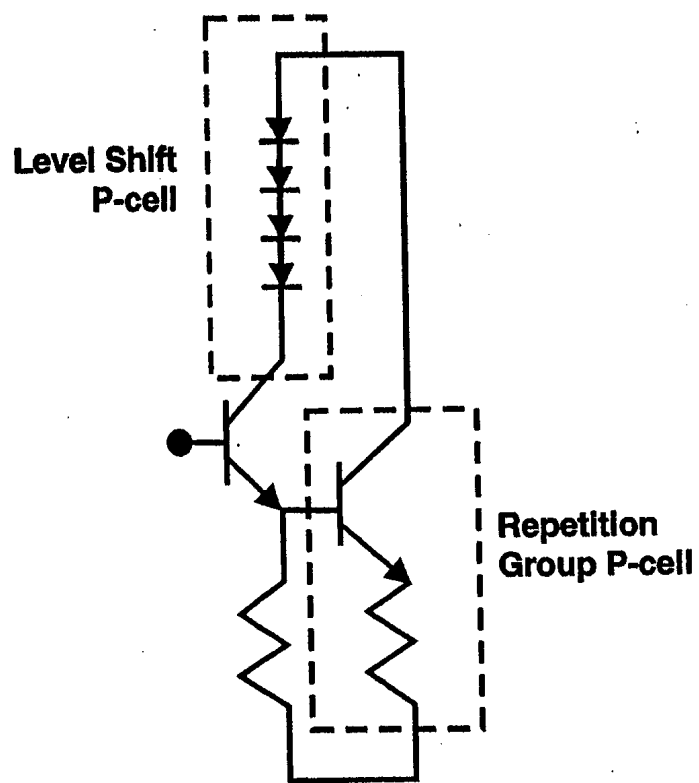
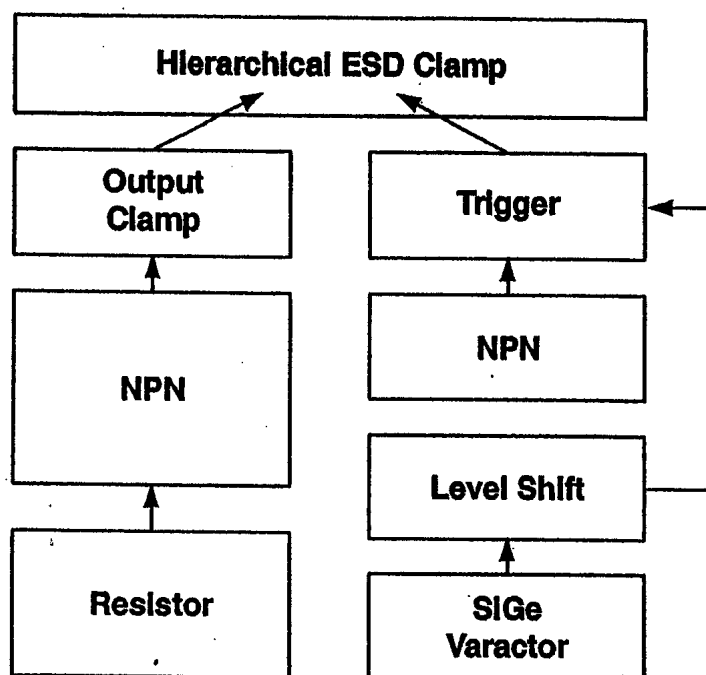


Figure 15



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Figure 16



Schematic Design System

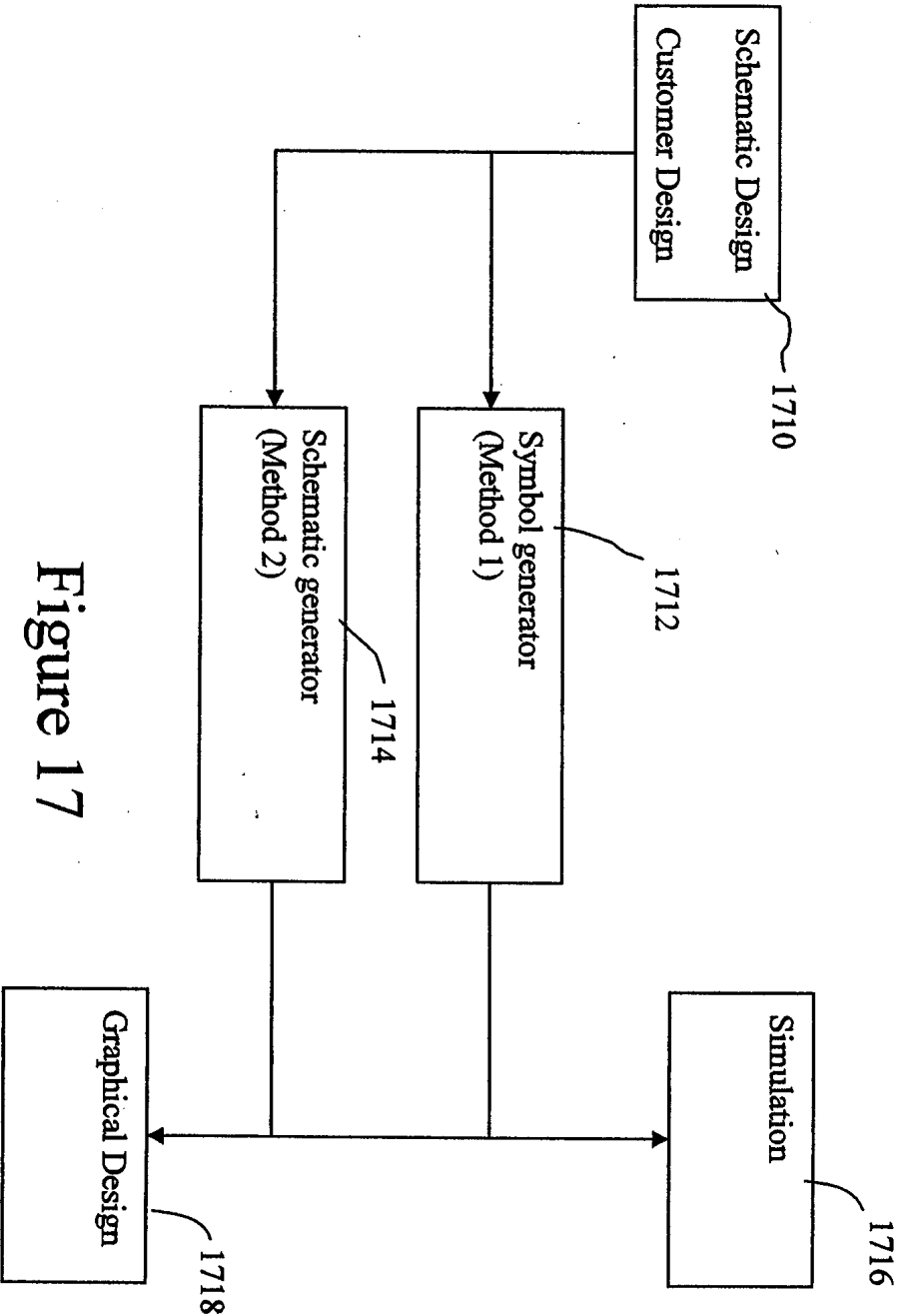


Figure 17

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Symbol and Schematic

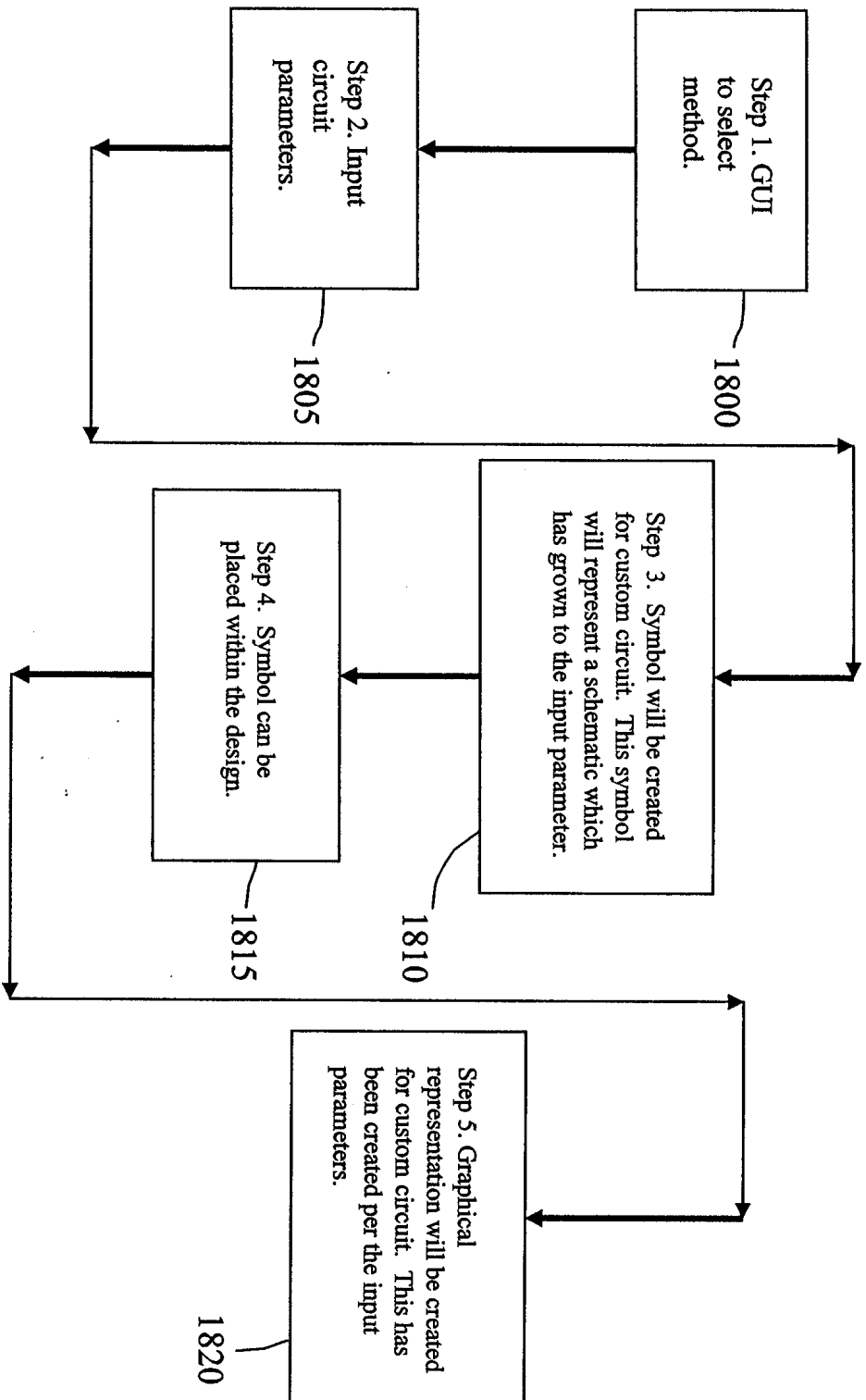


Figure 18

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Schematic Method 2

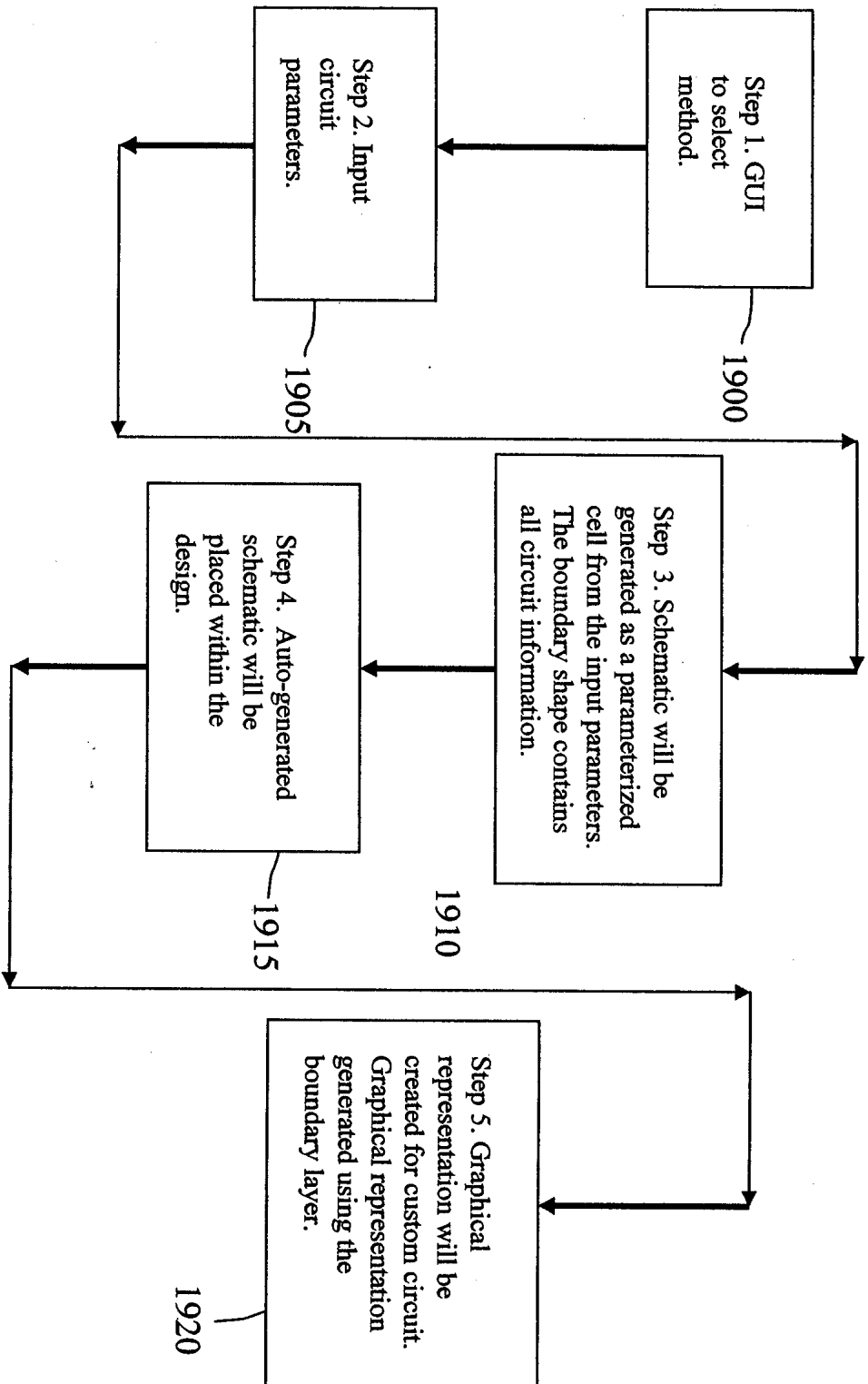


Figure 19

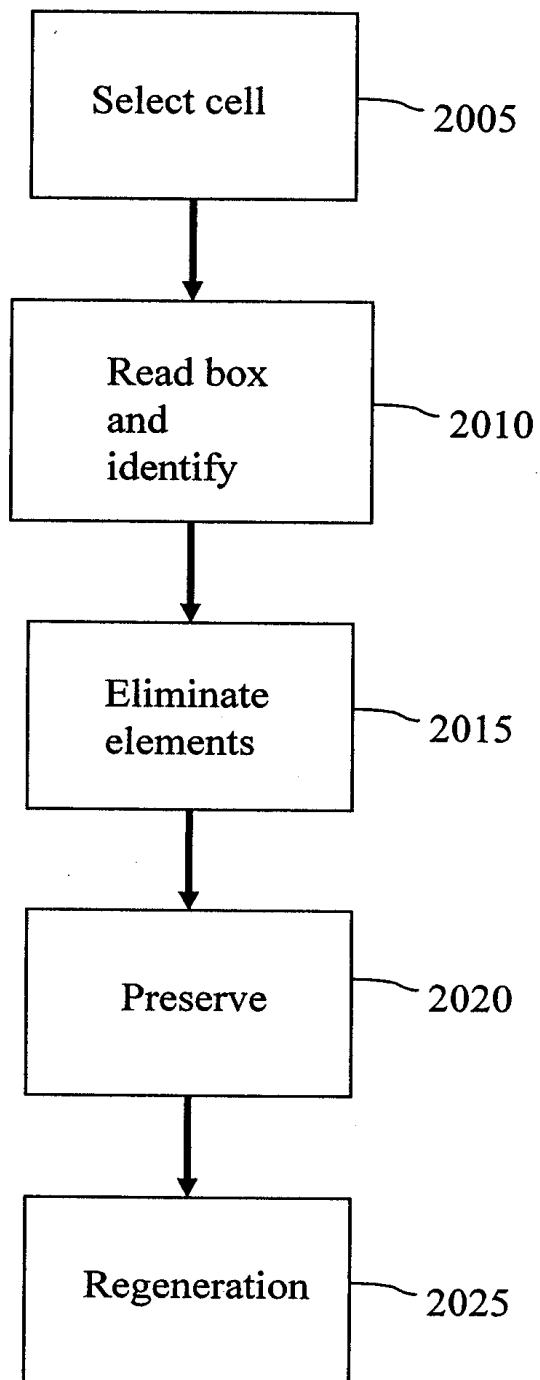


Figure 20

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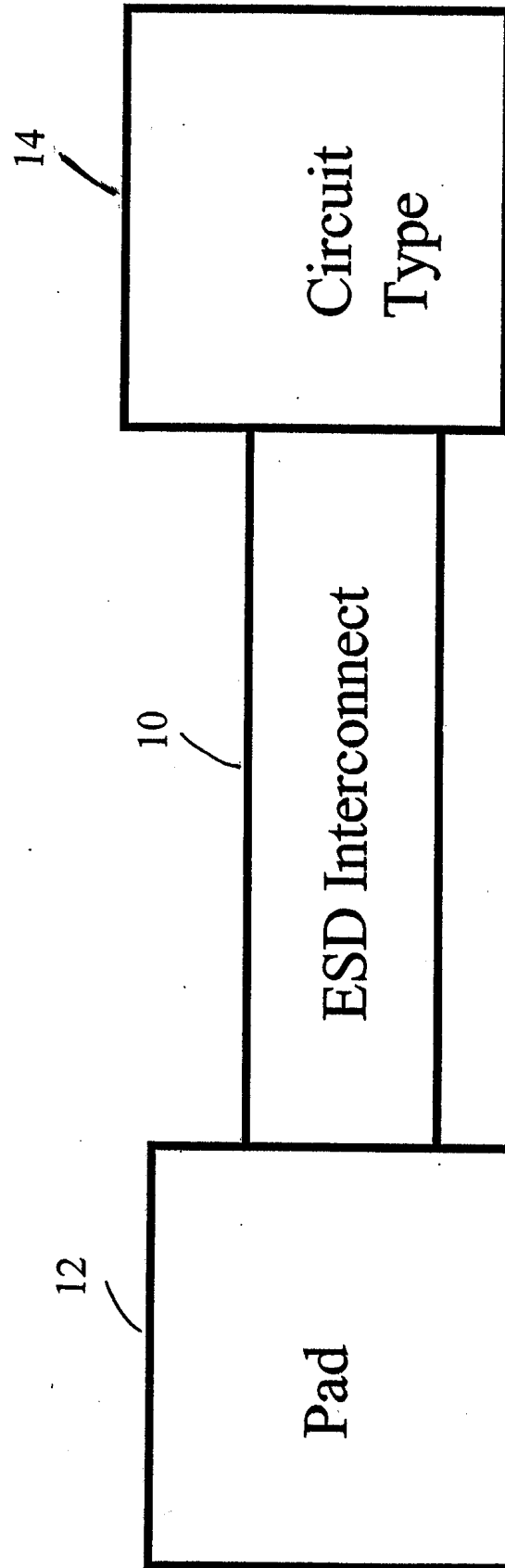


Figure 21

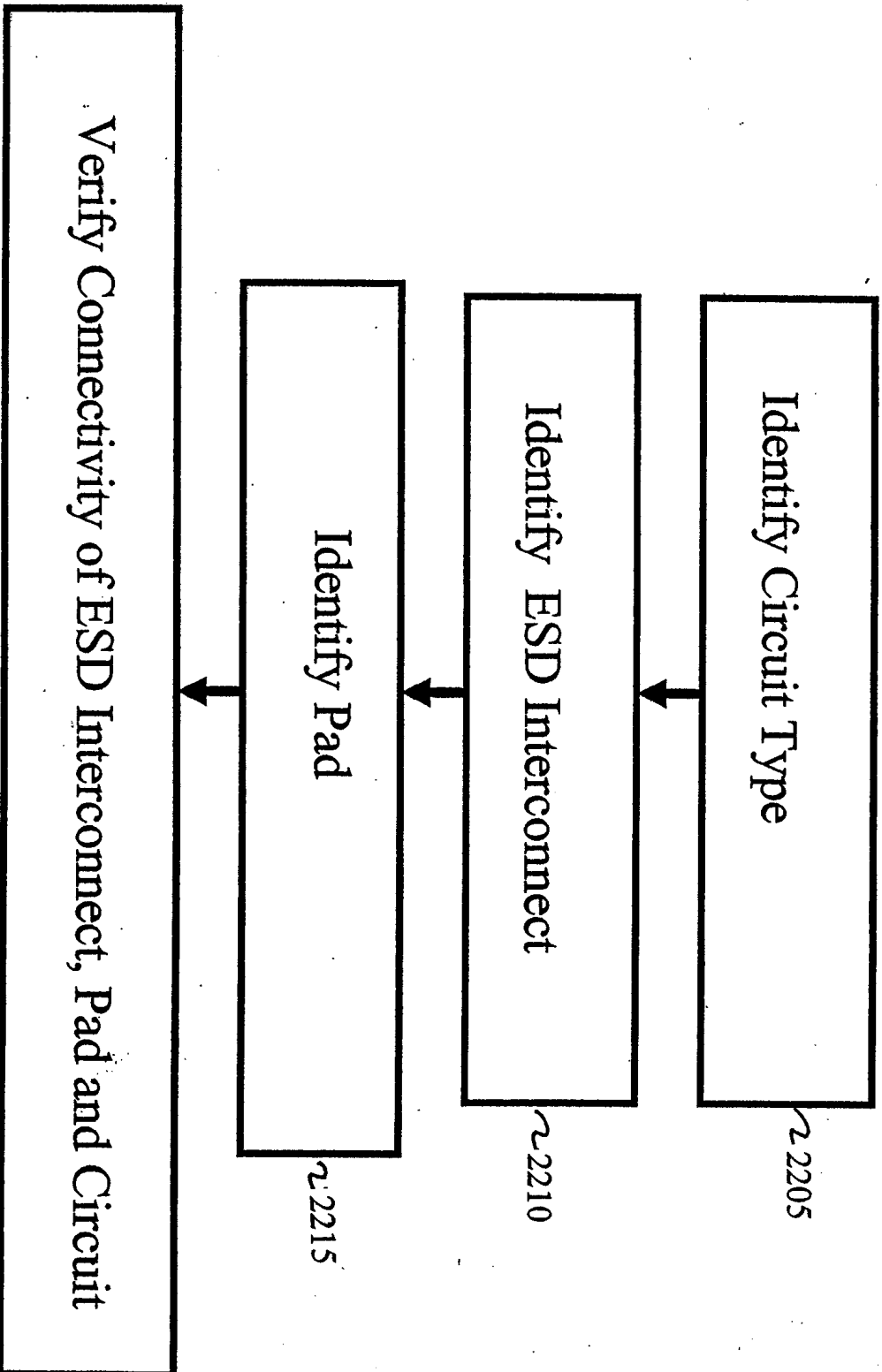


Figure 22

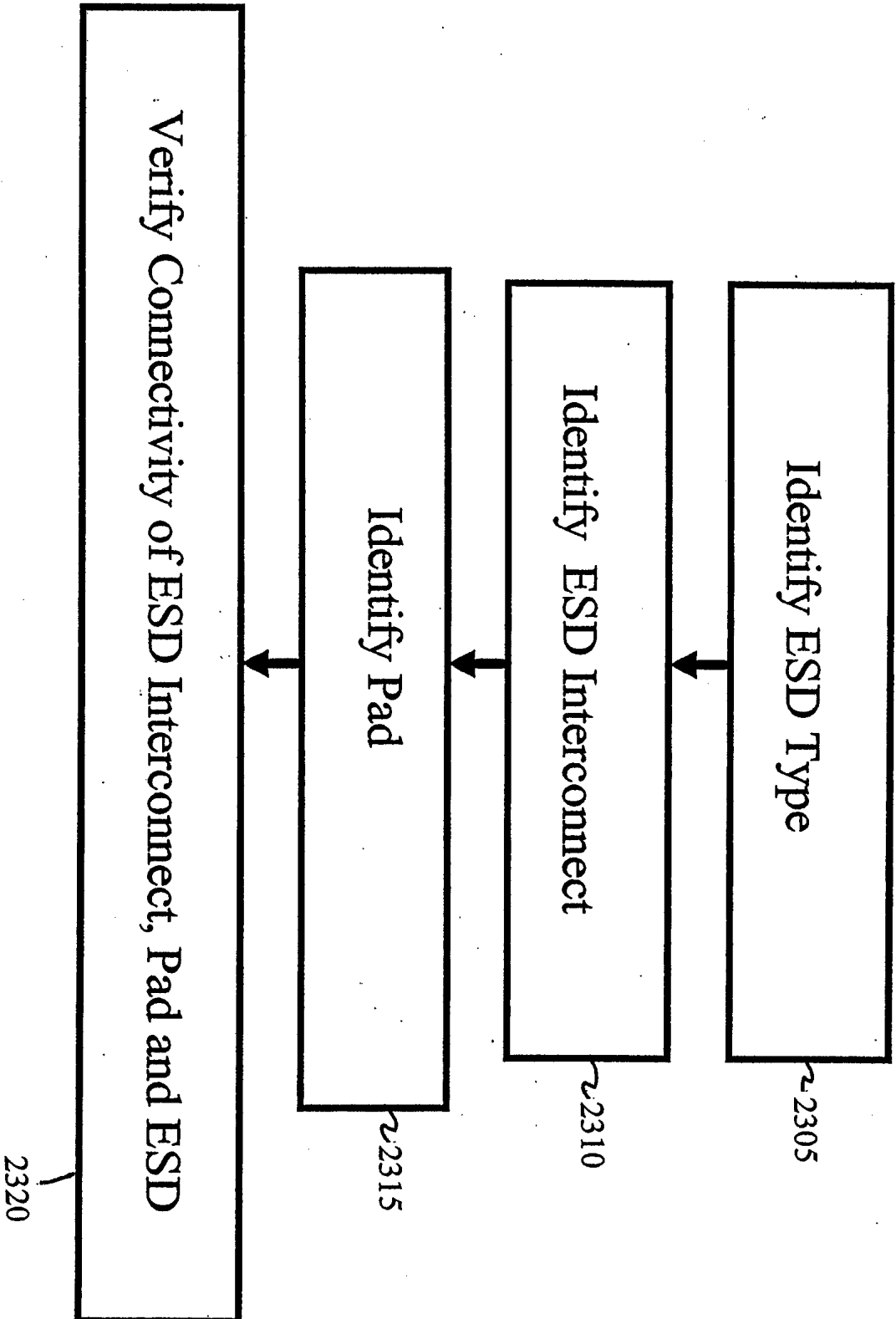


Figure 23

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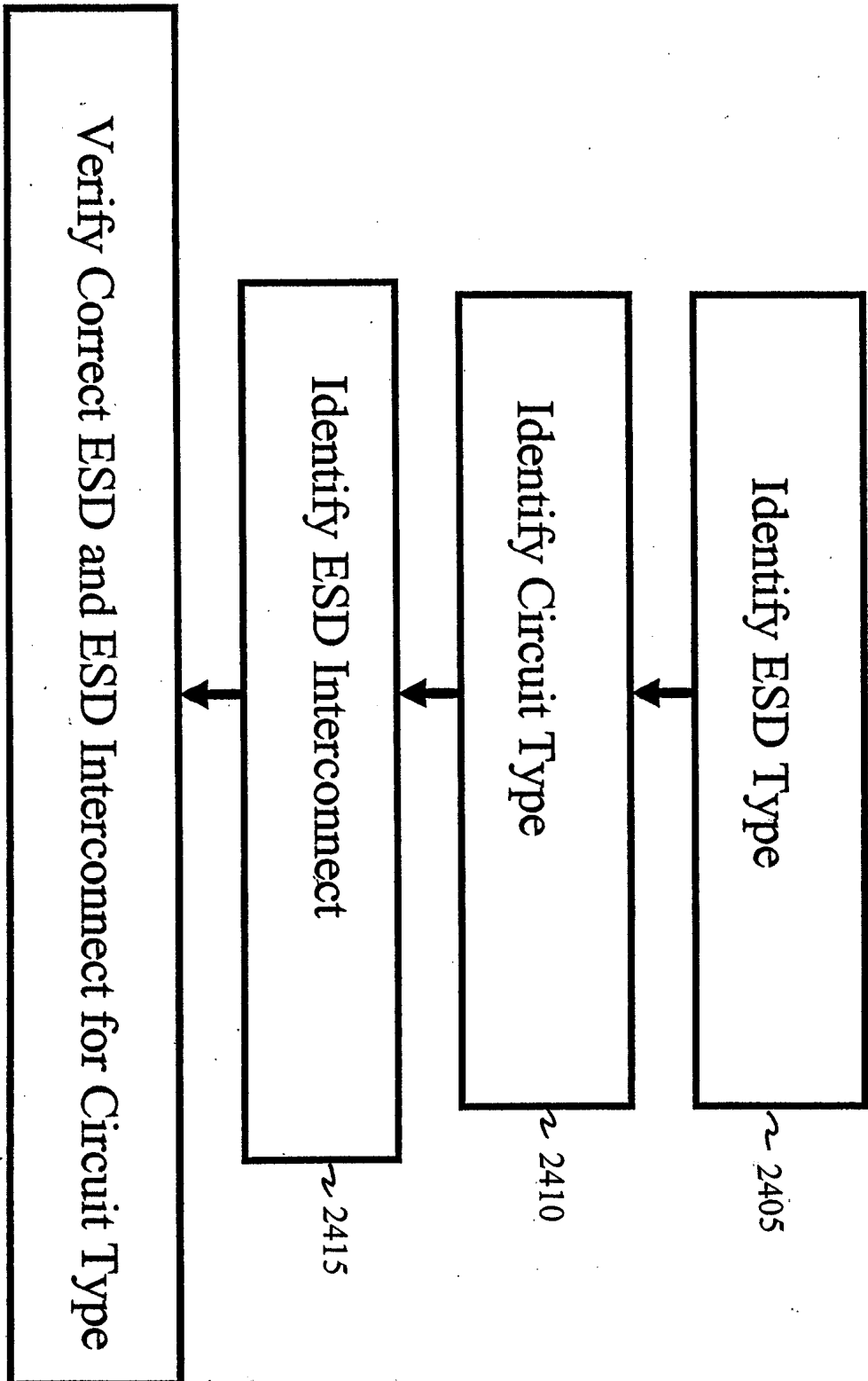


Figure 24

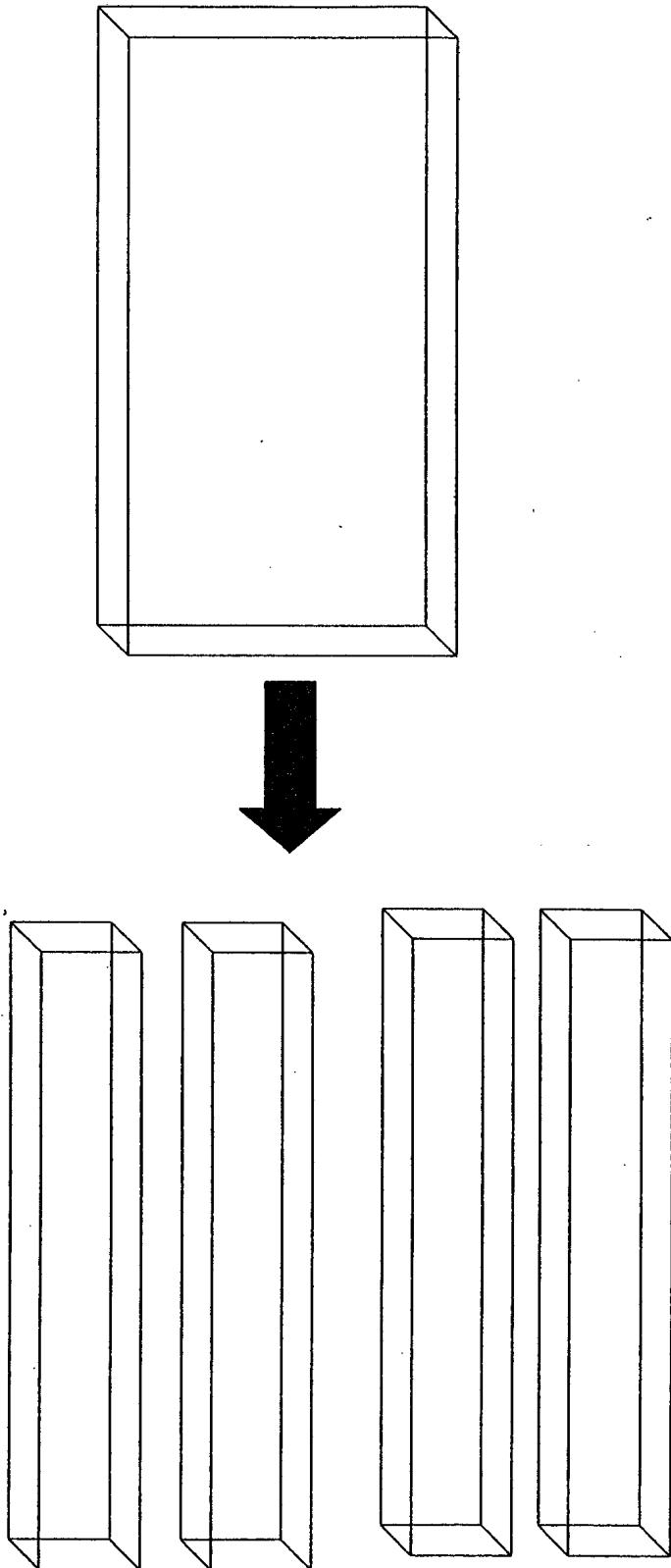
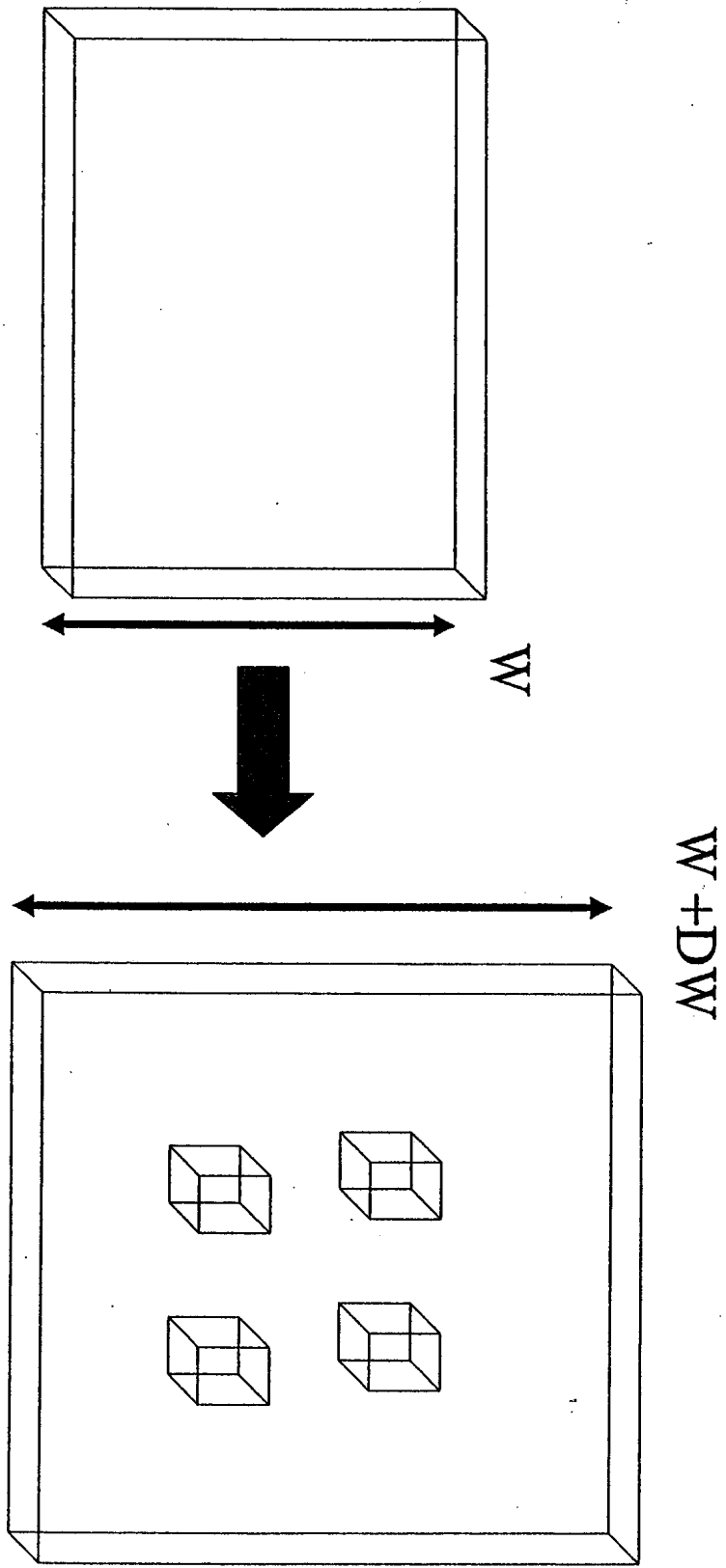


Figure 25

ESD Interconnect P-Cell : Ballasting Feature in P-Cell
to provide Current Uniformity

Figure 27



ESD Interconnect P-Cell : Cheesing Feature widening of
metal in P-Cell for ESD robustness

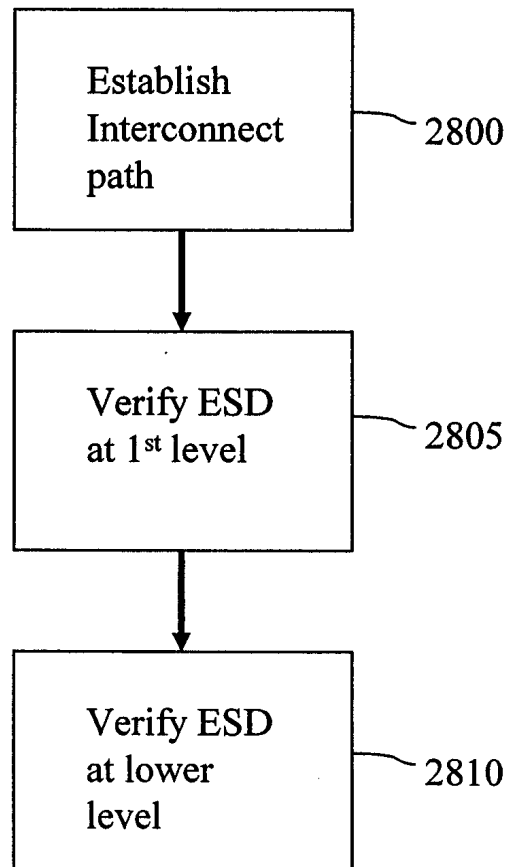
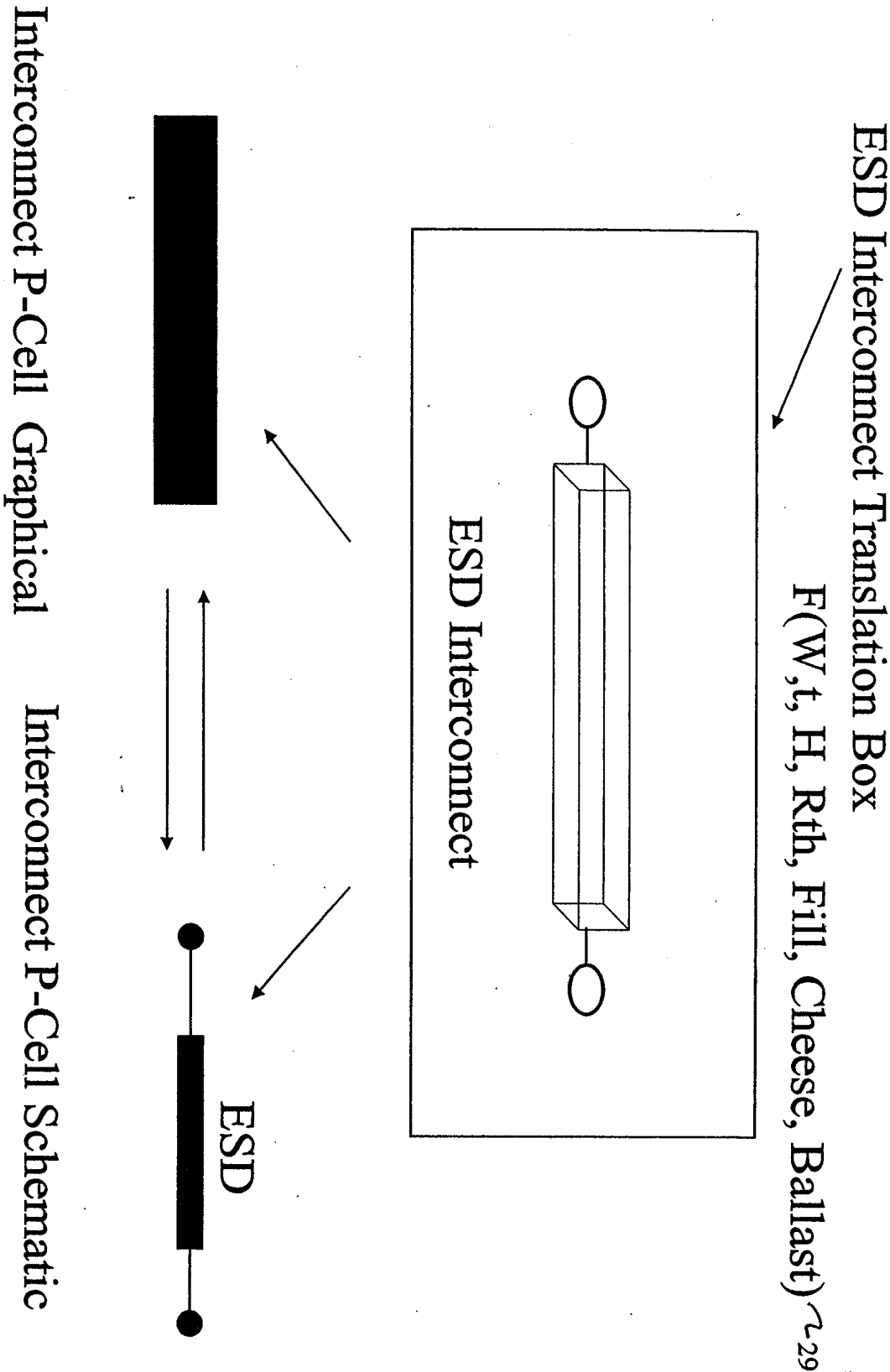


Figure 28



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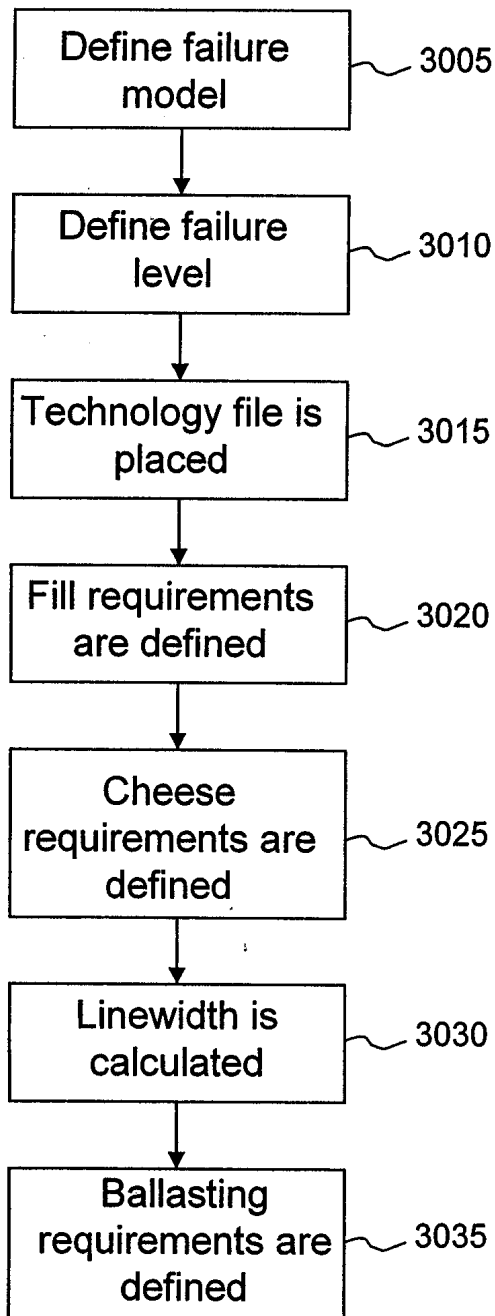


Figure 30a

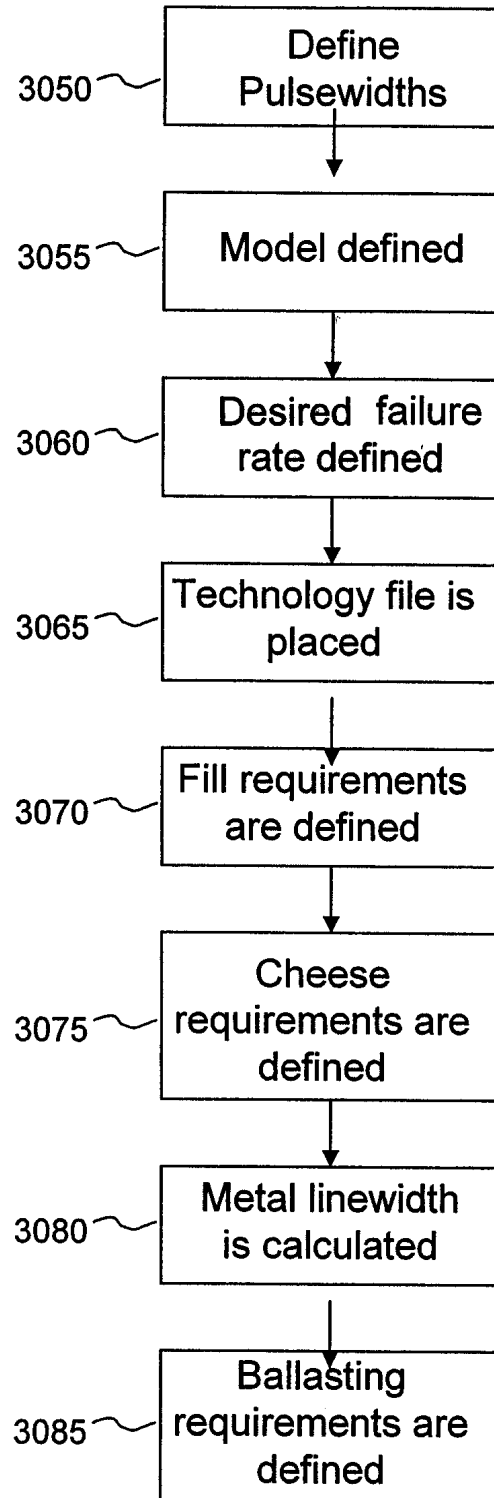


Figure 30b